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JUN 79 R W BRODERSEN , D A HODGES DAAG29-76-G-0244
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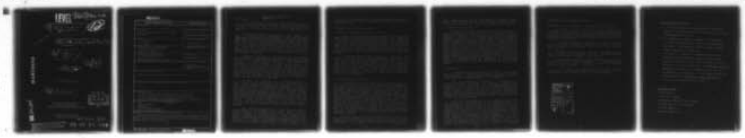

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(10) R. W. Brodersen
D. A. Hodges

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ELECTRONICS RESEARCH LABORATORY
COLLEGE OF ENGINEERING
UNIVERSITY OF CALIFORNIA, BERKELEY 94720

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Research has been carried out on real-time signal processing using techniques amenable to realization in large-scale integrated circuit technology. Specific system elements studied include precision frequency filters, multiplying digital-analog converters, and correlators.

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Introduction

U.S. Army Research Office Grant DAAG29-76-G-0244 supported research in the Electronics Research Laboratory, University of California, Berkeley, from 15 June 1976 through 14 June 1979 under the title "On-Chip Peripheral Circuits for CCD signal processors."

The problem studied in the course of this research was that of real-time signal processing of analog signals using large-scale integrated circuit technology. There are important requirements for real-time signal processing in many defense systems. Examples are sonar and radar detection systems, and voice, video, and digital data communication systems. Although there has been a strong trend toward digital signal processing in recent years, many instances still exist for which the necessary signal processing specifications can only be met, or can most economically be met, with the use of some analog electronic signal processing techniques.

Important objectives of this research were to determine the limitations on analog signal processing in standard LSI technologies, and to find means of improving on the performance and versatility of analog LSI signal processors. The use of LSI technology is highly desirable for most defense systems. The advantages include smaller size and weight, improved reliability, and reduced power consumption. In the past, large scale integration of analog signal processing functions was inhibited by the need for many off-chip components, often with tight requirements on matching and stability. Our research has demonstrated a number of new techniques for analog LSI design which drastically reduce the need for off-chip components.

Initially our attention was on charge-coupled device (CCD) filters, and on the amplifiers and other circuits needed to permit fully-integrated LSI filters and correlators. During the course of our research, it became clear that there are alternative techniques for realization of these functions which are preferable to CCD techniques in many cases. The CCD filters still have important specialized applications as matched filters, linear-phase filters, and comb filters; but a great many low pass, bandpass, and bandstop filter requirements can be satisfied at lower cost and with better specifications using the switched-capacitor ladder filters developed in the course of this research. The ease with which switched-C filters may be digitally programmed makes them highly attractive elements in adaptive systems.

Only metal-oxide-semiconductor (MOS) LSI technologies were considered in this research, for several reasons. Charge-coupled devices are achieved only in MOS. This research has helped to demonstrate the availability of other necessary elements of analog signal processing systems in standard MOS technologies, including amplifiers, multipliers, digital-to-analog converters, etc. Another consideration is that digital circuit functions are realized at high density in MOSLSI processes; this

is important because practical LSI signal processing systems are virtually certain to employ a combination of analog and digital circuit functions.

Important results of this research

1. Low-noise operational amplifiers in MOSLSI.

Prior to this research, the only operational amplifiers demonstrated in standard MOSLSI had electrical noise levels and power consumption so high as to severely limit their usefulness in complex, critical signal processing systems. A careful study of the noise sources in MOS amplifiers was made. Device measurements were made and fit to the noise model in program SPICE (a widely-used circuit simulator developed at Berkeley with ARO and other support). Design guidelines were established to achieve minimum amplifier noise within the constraints of a given MOS process.

A high-performance NMOS operational amplifier was designed with the aid of the understanding developed in the initial study. Noise, power consumption, and chip area were all much smaller than for previous designs. Additional features are fully internal frequency compensation and low output impedance with wide dynamic range. Thorough measurements confirmed the validity of the design approach. This amplifier has been the basis for a number of additional designs for various requirements, both at Berkeley and elsewhere. Publications on this work are listed in the Appendix.

2. Switched-capacitor filters.

A study of alternative techniques for preventing aliasing or foldover distortion in CCD filters led us to the concepts of the switched-capacitor ladder filter. These filters employ ratioed MOS capacitors, MOS transistor analog switches, and MOS transistor operational amplifiers together with a precise digital clock signal to create precision audio-frequency filters. In many instances the switched-C filter can perform the complete filtering function, with no need for a CCD at all. The advantages of eliminating the CCD include greater dynamic range due to the small insertion loss, simpler prevention of aliasing due to higher sampling frequency, and reduced harmonic distortion due to elimination of the effects of nonlinear parasitic capacitances. Important concepts which were pioneered with ARO support on this grant are the ratioed-capacitor method for adding transmission zeros to the filter transfer function, and the lossless digital integrator technique for eliminating excess phase in the switched-C filters.

To date, fully-integrated switched-capacitor filters have demonstrated untrimmed gain accuracy of ± 0.1 dB, center frequency accuracy of 1%, and 90 dB of dynamic range for operation at audio frequencies. There appears to be no barrier to extending the

useful frequency range to the low megahertz frequency range, based upon standard NMOS and CMOS LSI processes. Publications and reports documenting our research are listed in the Appendix.

3. Frequency-locked filters.

Exploratory studies have been made on the feasibility of fully-integrated MOS filters based on frequency-lock and/or phase-lock techniques. In this approach (as for switched-C filters,) a quartz crystal provides a precise, stable frequency reference which is used in a phase-locked loop to stabilize center frequency. For high-Q applications, a separate feedback path is desirable to stabilize gain or Q factor. The elements of these filters are continuous time active integrators and active multipliers. Because of the continuous-time character of the entire filter, there is no sampling and no aliasing problem. Detailed studies of a 455 kHz filter with a Q of 60 and a gain of 36 dB show that it should be realizable in a standard MOSLSI process. High-Q filters for use at frequencies above 100 kHz are probably smaller in die area and more stable using this technique rather than the switched-capacitor approach. We were in the midst of detailed design and simulation of a monolithic frequency-locked filter as the term and funding under this grant ended.

4. Correlators.

Correlators and autocorrelators are needed in many signal detection systems. Although CCD structures can perform correlation functions, a major drawback is that implementing variable coefficients in a fully-integrated CCD is difficult.

We have studied the feasibility of implementing a variable-coefficient correlator via alternative MOSLSI techniques. An N-tap correlator requires N multiplications to be performed in each sampling interval. These can be performed with either analog or digital multipliers. The first approach requires an analog delay line and accurate 4-quadrant analog multipliers, and is not easily implemented in LSI form. Fast digital multipliers are available, but are very large in chip area and consume a great deal of power.

An alternative approach is to use a digital delay line and perform the multiplications with a multiplying digital to analog converter. The latter element has been successfully realized in MOSLSI through earlier work in our laboratory; it employs a binary-weighted array of integrated MOS capacitors. A multiplication is completed in 0.2 to 1 microsecond (depending on design details) with 8 to 12 bit coefficient accuracy. Coefficients are stored digitally in read-write memory. In the correlator application the multiplier can be time-shared. A breadboard correlator in this form was constructed in our laboratory. It performs autocorrelation on ten stored samples within a 125 microsecond sampling interval with a measured 66 dB dynamic range. Monolithic realization would lead to significant

improvements in these specificatiions.

Applications of this research in Army and other DoD programs

The remote monitored battlefield sensor system, under development by Ft. Monmouth with RCA Advanced Communications Laboratory as contractor, is using switched-capacitor filters in its signal preprocessing which precedes microcomputer-based final processing. Further use of analog signal processing is anticipated for future systems.

Low power analog signal processing is needed for sensors in munitions fuzes. AARADCOM is sponsoring work by RCA for the Army, in which switched-capacitor filters are a strong candidate for application.

Phased-array hydrophones are under development for the Navy by Hughes Ground Systems Division. Switched-capacitor filters are extensively employed in this system.

Work on fully-integrated channel vocoders is being sponsored by DARPA at Texas Instruments. A combination of CCD filters and switched-capacitor filters are employed in the MOSLSI prototype system developed in this project.

In each of the four cases itemized, upon request from the contractors we have given suggestions, advice, preprints of our publications, etc. to assist them in their developments.

Publications sponsored by ARO

1. G. M. Jacobs, "Practical design considerations for MOS switched capacitor ladder filters," Masters Project, University of California, ERL Memorandum M77/69, Nov. 1977.

2. R. W. Brodersen, P. R. Gray, D. A. Hodges, D. J. Allstot, and G. M. Jacobs, "Switched-capacitor filters for telecommunications applications," 1978 European Conf. on Circuit Theory and Design, Lausanne, Switzerland, 4-8, Sept. 1978.

3. G. M. Jacobs, D. J. Allstot, R. W. Brodersen, and P. R. Gray, "Design techniques for MOS switched capacitor ladder filters," presented at the ISCAS'78 Special Session on Miniaturized Filters, New York, 17-19 May 1978, and published in the IEEE Trans. on Circuits and Systems, vol. CAS-25, no. 12, December 1978, pp. 1014-1021.

4. D. Senderowicz, D. A. Hodges, and P. R. Gray, "High-performance NMOS operational amplifier," IEEE Journal of Solid-State Circuits, vol. SC-13, no. 6, December 1978, pp. 760-766.

Personnel Supported

S. Lum, MSEE 6/79

T. Choi, M.S. Candidate

D. Senderowicz, MSEE 12/77; Ph.D. Candidate

R. Fellman, MSEE 6/77; Ph.D. Candidate

G. Jacobs, MSEE 12/77

Cynthia Ott, MSEE 12/76